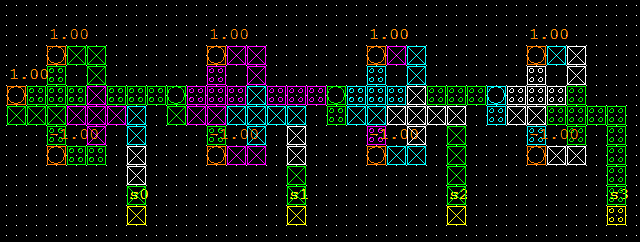
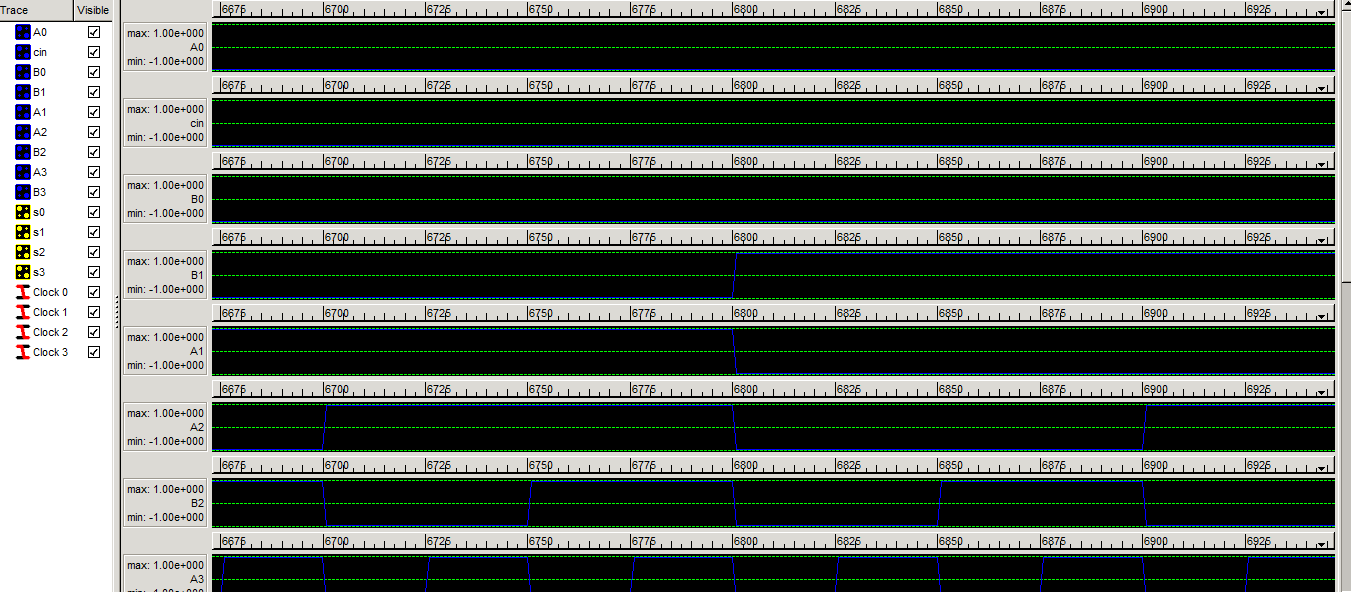
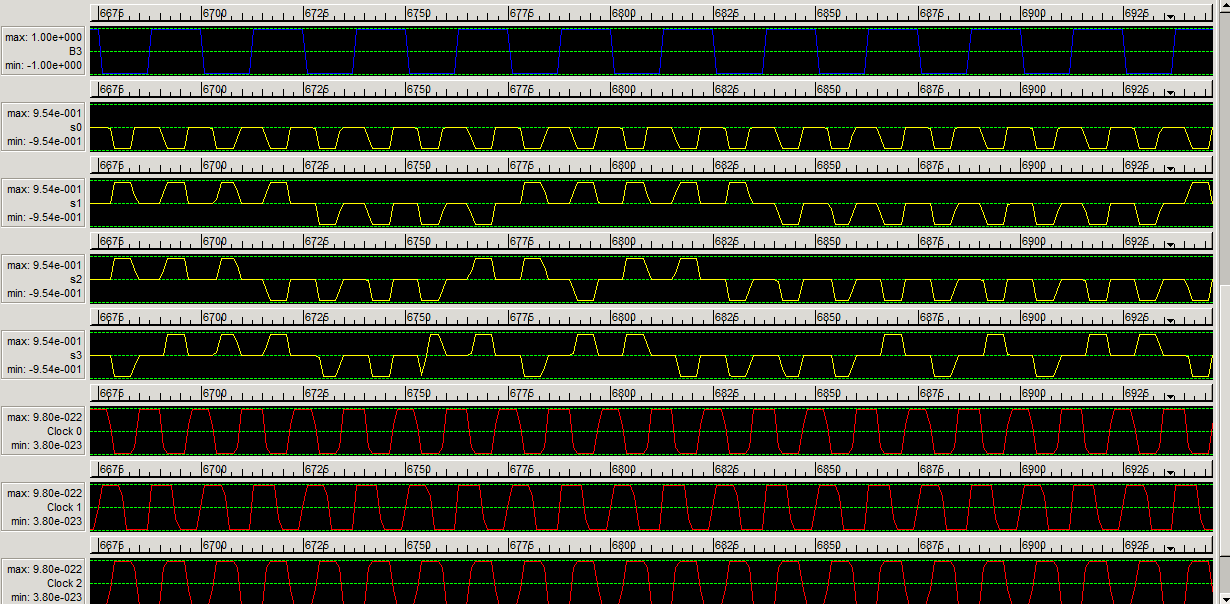
**4 bit ripple carry adder:**

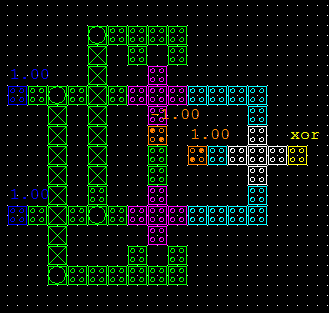


Simulation Results:

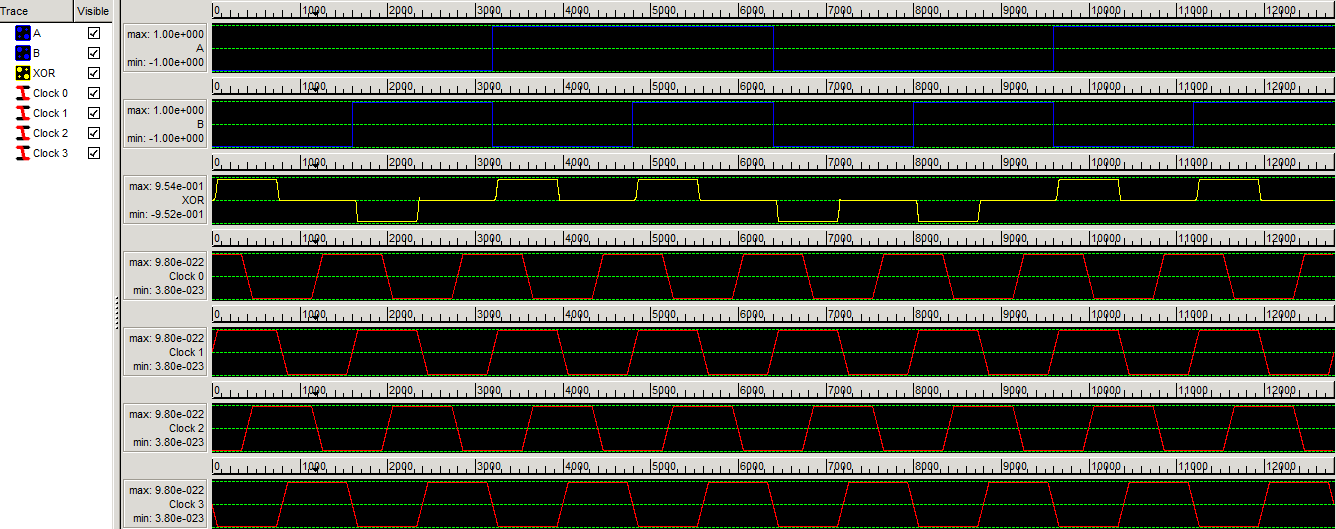




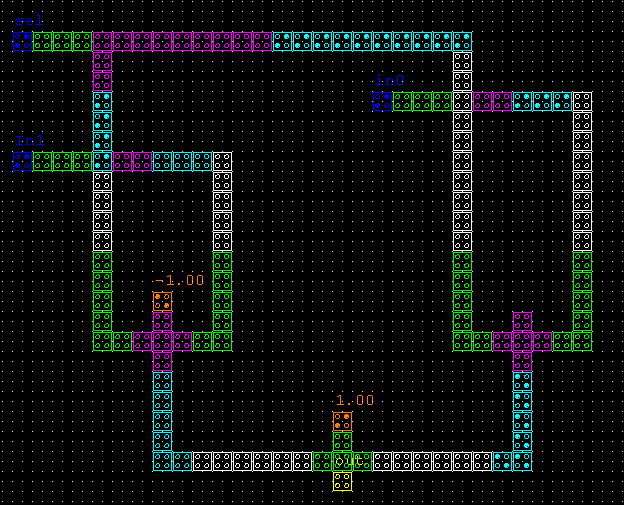
**Xor gate:**

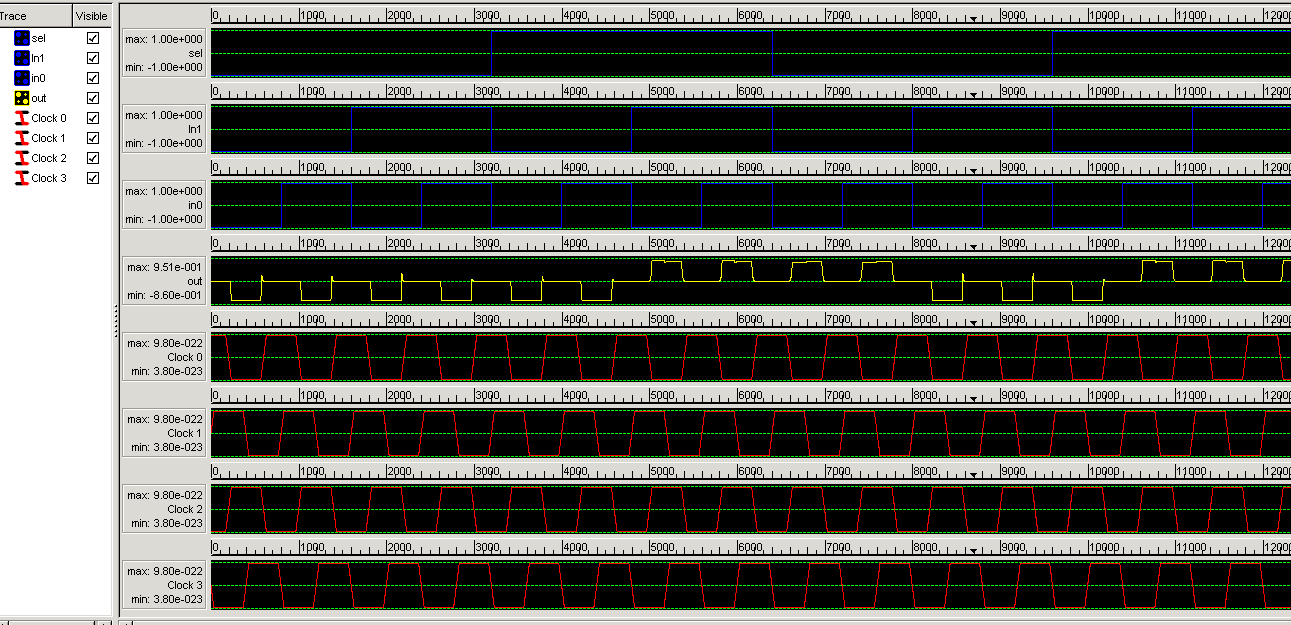
****

Simulation Results:

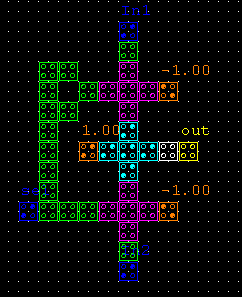


**2:1 Mux:**

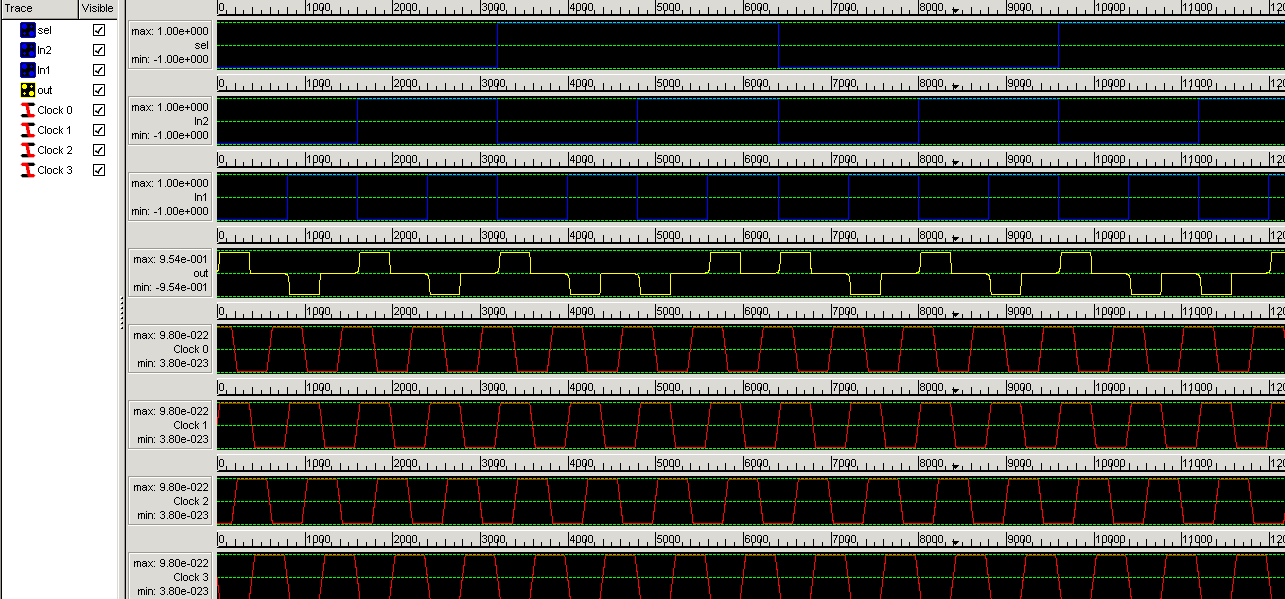


Simulation Result:  


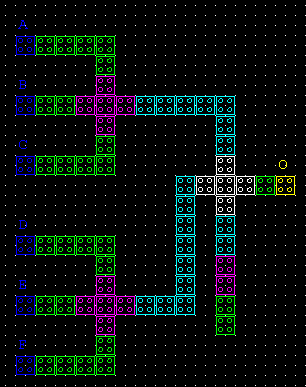
**Multiplexer:**



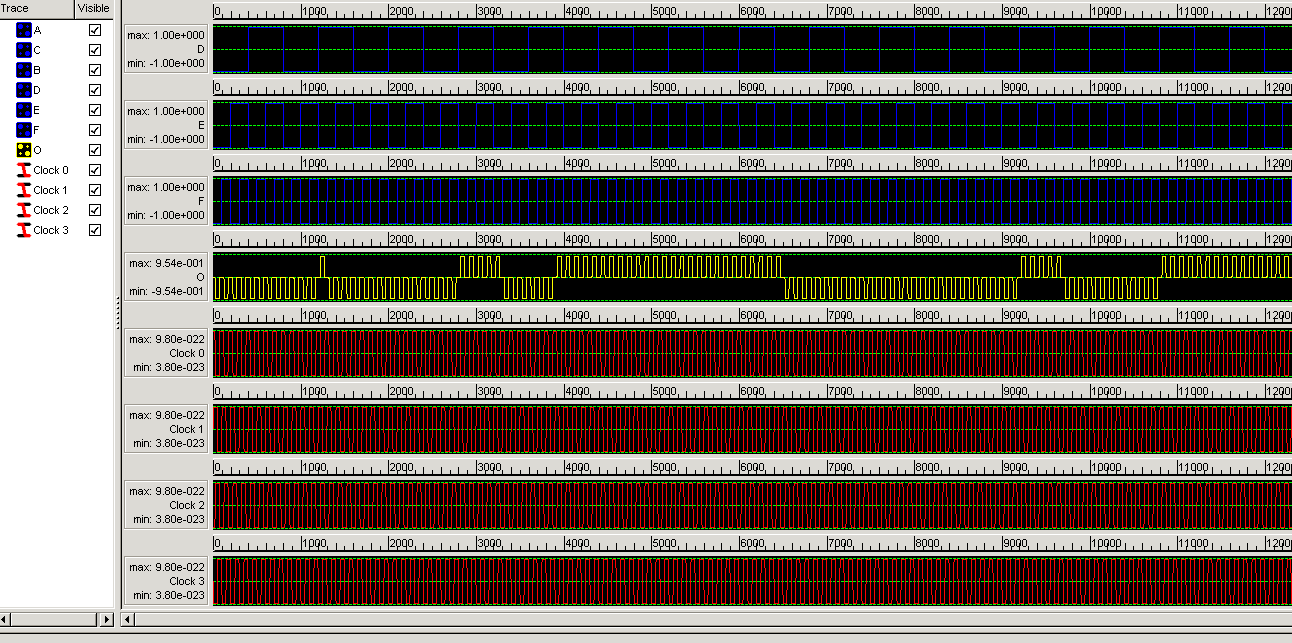
Simulation Results:



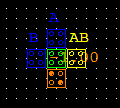
**Majority circuit:**



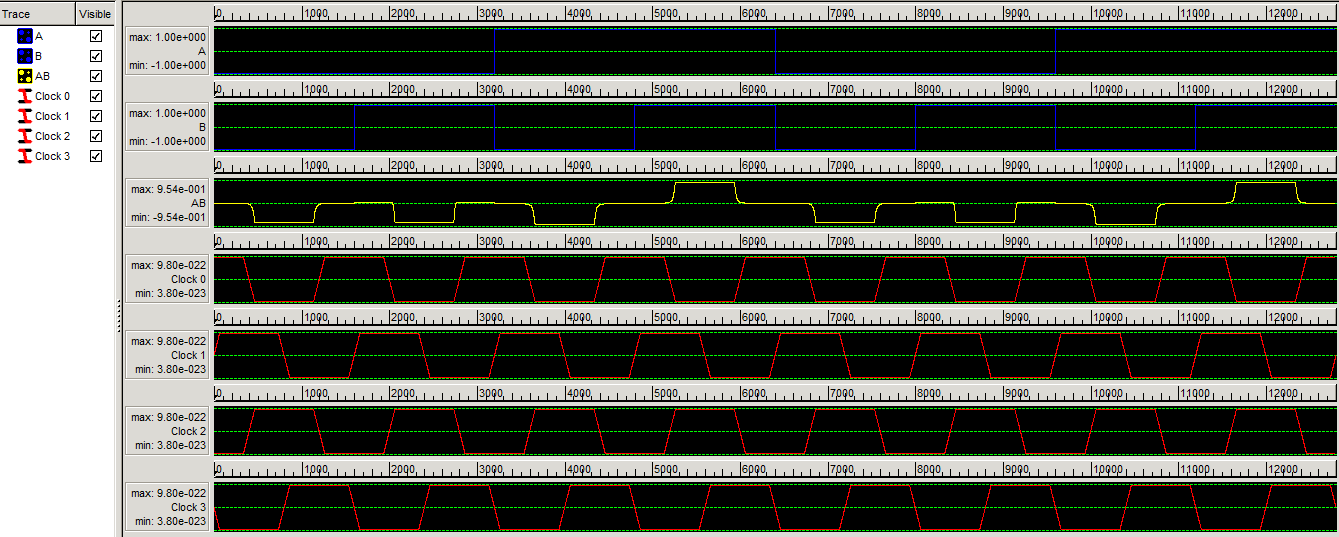
Simulation Result:



**AND GATE:**

****

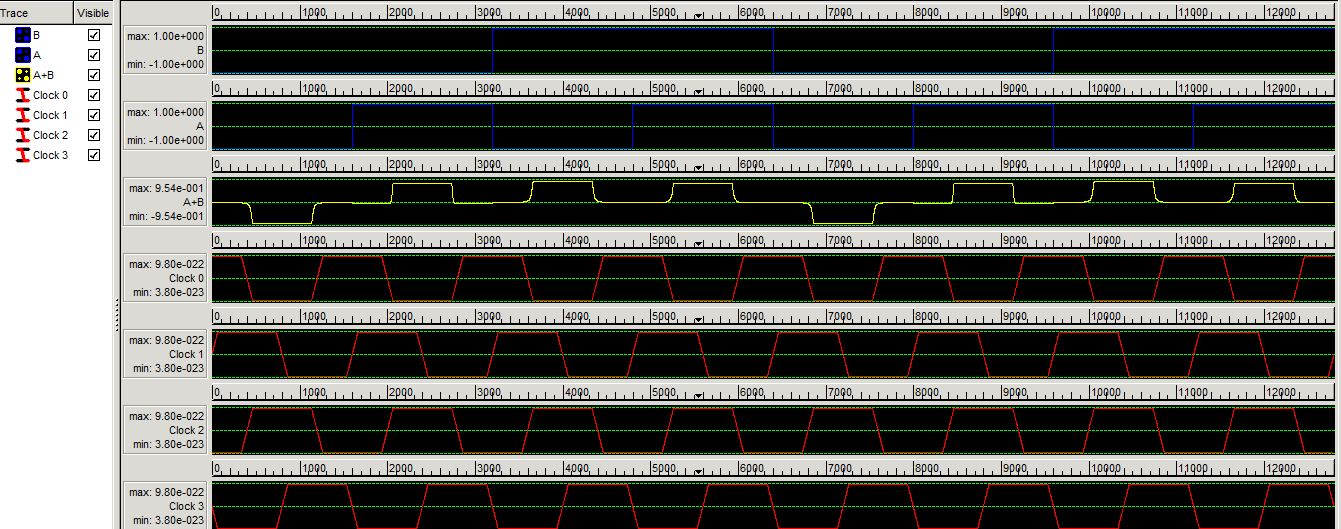
Simulation Results:



**OR GATE:**



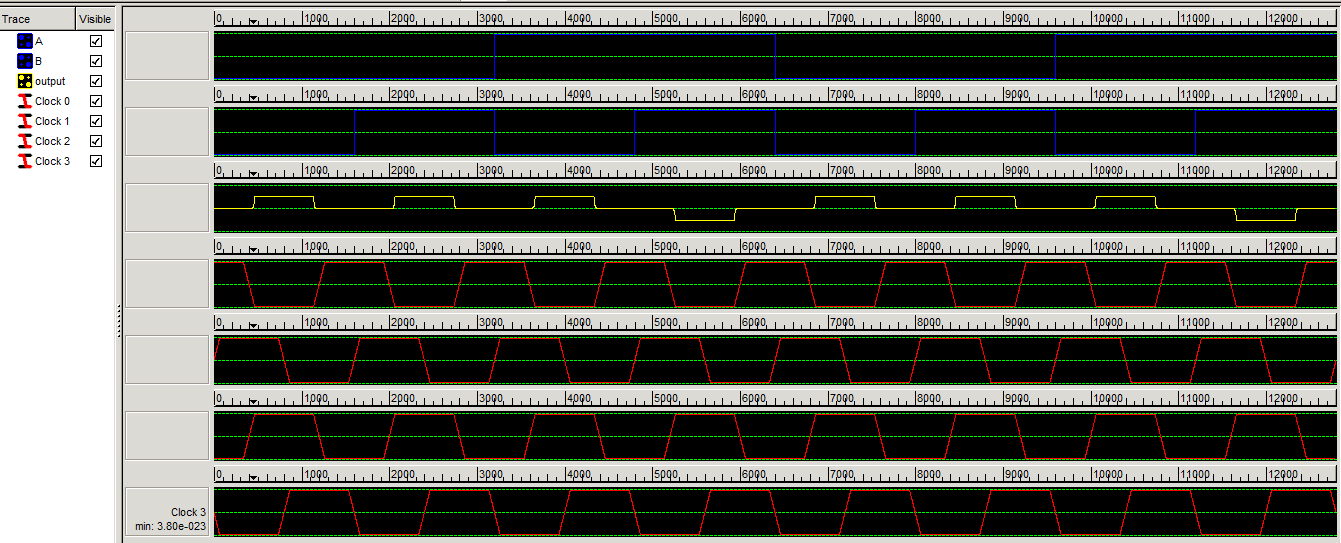
Simulation Results:



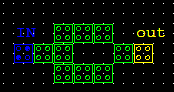
**NAND GATE:**



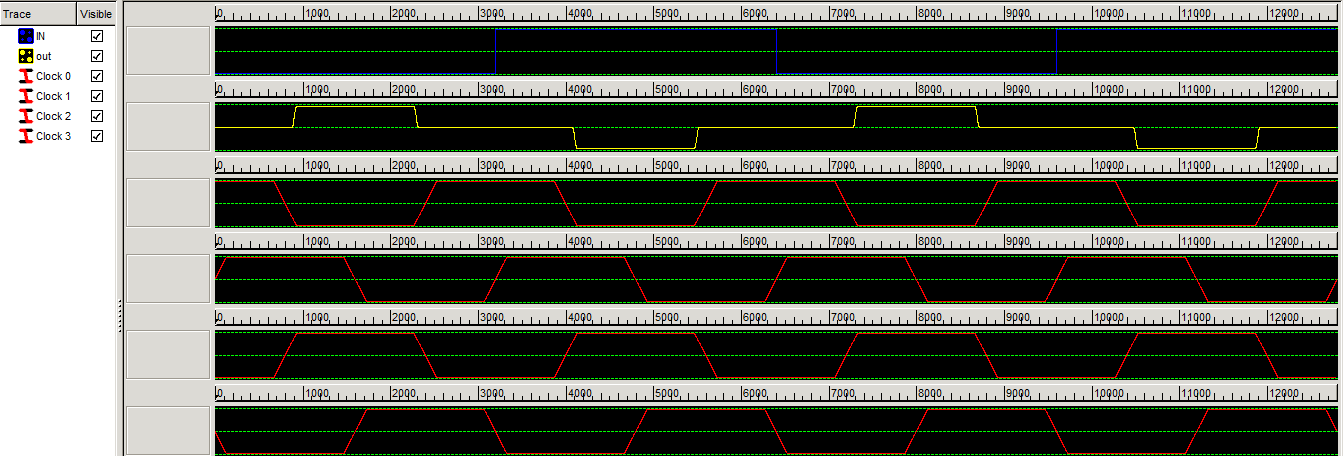
Simulation Results:



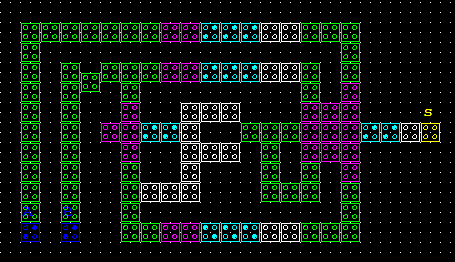
**INVERTER:**



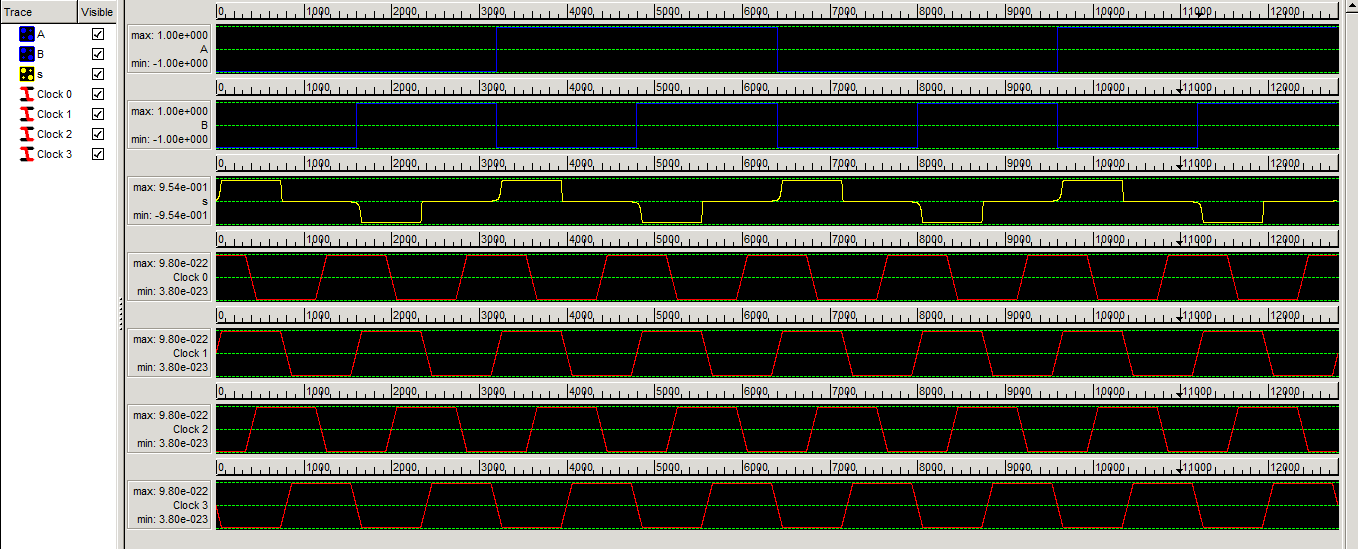
Simulation Results:



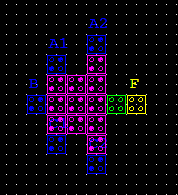
**SERIAL ADDER:**

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Simulation Results:



**FIVE I/P MAJORITY GATE:**



Simulation Results:

